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# Phase Logic Based on $\pi$ Josephson Junctions

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The transition to Josephson digital circuits with the representation of information in the form of phase jumps of the superconducting order parameter on heterostructures promises a radical increase in the degree of integration while maintaining high speed and energy efficiency. However, it is not yet possible to manufacture reproducible bistable Josephson junctions, which are necessary for the functioning of the previously proposed basic units of the phase logic. To solve this problem, the concept of phase logic based on  $\pi$  junctions is proposed and analyzed within the resistive model of Josephson heterostructures. The potential energy of such junctions has a single minimum, with a difference in the order parameters of the electrodes equal to  $\pi$ . It is demonstrated that the use of  $\pi$  junctions allows one to implement the entire set of logic devices necessary for the operation of digital computing devices based on phase logic.

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# **INTRODUCTION**

Digital superconducting electronics, using the features of the Josephson effect and macroscopic quantum interference in superconducting circuits, allows one to create advanced analog-to-digital and digitalto-analog converters, decimation filters, time measuring systems, correlators, and arithmetic logic devices with unique performance and energy efficiency [1-12]. With a typical clock frequency of 20 GHz, the dynamic dissipation power per Josephson junction can be increased to 13 nW [2]. Josephson devices can also help dealing with superconducting quantum computing systems [13–18].

For the wide application of digital circuits based on fast single-quantum (FSQ) logic with the representation of information in the form of the presence/absence of a magnetic flux quantum  $\Phi_0$  in the superconducting circuit of a logic cell, it is critically important to reduce their characteristic dimensions. Existing estimates [19] for the maximum element density in circuits using geometric inductance for information storage and superconducting "strips" for connections provide about 10<sup>7</sup> Josephson junctions per square centimeter. Further reduction of the planar dimensions of cells and distances between them is problematic because of the almost exponential growth of mutual inductances and crosstalk. The problem of miniaturization is especially significant in Josephson circuits intended for operation at ultralow temperatures in hybrid quantum-classical computers, where it is necessary to reduce the critical current of heterostructures in order to avoid excessive heating of the cryogenic system.

A promising solution to this problem is the transition to the so-called *phase logic*, which is based on two basic principles:

-Information is stored in the phase of the bistable Josephson element rather than in the presence/absence of a magnetic flux quantum in the basic cell.

-Circuit solutions are free of connecting inductances; i.e., electrical circuits contain only Josephson junctions.

A pair of logic states 0 and 1 can be obtained even using a single bistable Josephson junction [20-24]. In this case, the information-storage element of logic devices is reduced to this single junction. Its state is determined by which of the two energy minima corresponding to the phase jump of the order parameter (element phase)  $\phi = \phi_0$  or  $\phi = \phi_1$  it is currently in. The information propagation corresponds to the wave of the phase change in the superconducting order parameter rather than to the propagation of the fluxon.

The proposed approach was used to develop compact, energy-efficient circuits for the practical implementation of phase logic and memory [25, 26]. It was demonstrated that the characteristic planar dimensions of digital devices can be an order of magnitude smaller than traditional FSQ implementations (the area on the chip for an 8-bit adder can be reduced from more than 200 to  $22 \,\mu m^2$ ) [25]. Unfortunately, to date, the manufacture of bistable Josephson junctions with specified and reproducible parameters is only at the development stage.

In this work, we demonstrate that workable digital phase logic circuits can be designed on the basis of combinations of 0 and  $\pi$  junctions (with a current—phase dependence shifted by  $\pi$ ), which provide the basic unit bistability necessary for this logic to work. It should be noted that the technology for manufacturing 0 and  $\pi$  junctions is well developed at present [27–31].

## GENERAL PRINCIPLES OF THE OPERATION OF PHASE LOGIC CIRCUITS

Figure 1 demonstrates the diagram of the basic unit of the phase logic on which elements with two stable physically distinguishable states are presented in the form of eight-pointed crosses, which correspond to phases of potential energy minima  $\varphi_0$  and  $\varphi_1$  $(0 \le \varphi_1 < \pi$  and  $\pi \le \varphi_2 < 2\pi)$ . Note the absence of inductances in the basic unit, which are intended to store magnetic flux quanta. In the supply Josephson transmission lines, all connecting geometric inductances are also replaced by Josephson ones.

Information in this basic unit is stored in the phase of the element  $J_m$ : its potential energy has two minima at  $\varphi = \varphi_1$  and  $\mathbf{e} = \varphi_2$ , respectively. The Josephson junctions  $J_{\text{in}}$  and  $J_{\text{out}}$  are the input and output ports of the circuit, respectively. The element  $J_l$  connects the information-storage element  $J_m$  to the output of the circuit  $J_{\text{out}}$ . Its parameters primarily affect the state reading mechanism. The bistable element  $J_v$  connects the input of the circuit to  $J_m$ , acting as a phase converter at the input of the unit.

Depending on the parameters of the phase converter (which can be either one bistable junction  $J_v$  or a serial connection of a pair of Josephson heterostructures [32]), the basic unit can perform all the modes necessary to implement the most common digital devices. Let us further consider the dynamic processes in the basic unit for the limiter mode, transmission line mode, and digital frequency divider mode.

In the *limiter mode* (top panel of Fig. 1), the incoming phase jump of the superconducting order parameter generates currents in the input cell, which lead to a phase change at the junction  $J_{in}$  and the converter element  $J_v$  by  $\sim 2\pi$ . However, the relation between the Josephson energies and the characteristic times of the processes for  $J_v$  and  $J_m$  is such that the phase converter switches between stable states before the information storage unit. The element  $J_m$  and the output cell remain in this mode in their original equilibrium states. The phase difference jump at the output of the



**Fig. 1.** (Color online) Basic unit of phase logic circuits on bistable contacts operating in the modes of (from top to bottom) limiter, transmission line, and digital frequency divider. The propagation of current and phase waves is shown by arrows.

unit is not formed. Sequential switching of Josephson junctions  $(J_{in})$  and bistable elements  $(J_v)$  is demonstrated by arrows in the top panel of Fig. 1.

In the *transmission line mode* (middle panel of Fig. 1), the converter  $J_v$  switches slowly, and the phase jump wave applied to the input creates a high current through it, changing the phases of the junction  $J_{in}$ , as well as the central element  $J_m$  and the output cell  $J_{out}$  by ~2 $\pi$ . In this case, the input pulse carrying the phase change by  $2\pi$  passes through the basic unit without changing its state. Sequential switching of Josephson junctions ( $J_{in}$ ,  $J_{out}$ ) and bistable elements ( $J_m$ ) is also demonstrated in the middle panel of Fig. 1 by arrows.

For intermediate values of the switching speed between stable states ( $\varphi_{0v}$  and  $\varphi_{1v}$ ) of the converter  $J_v$ , under the action of information coming to the input, the information-storage element  $J_m$  has time to change its phase from  $\varphi_0$  to  $\varphi_1$ . As a result, the status of the basic unit as a whole changes from 0 to 1; i.e., a write operation occurs. In the bottom panel of Fig. 1, this is indicated by half of the standard arrow. Note that the amplitude of the current pulse arising in the output cell ( $J_l - J_{out}$ ) after one wave of phase jumps arriving at the input is not enough to switch the junction  $J_{out}$ . However, after switching the basic element  $J_m$ , the state of the output cell changed: the current began to circulate in it (what can be used to read information). When the circulating current is added to the current



Fig. 2. (Color online) Basic unit of phase logic circuits based on  $\pi$  junctions, shown on the diagram by six-pointed crosses.

pulse caused by the next phase change wave applied to the input,  $J_{out}$  switches between its stable states (with phases 0 and  $2\pi$ ) and generates a phase change wave into the output line. In this case, the information-storage element  $J_m$  returns from the state 1 to the state 0. In the bottom panel of Fig. 1, this is indicated by the second half of the standard arrow. It can be concluded that the basic unit in this case operates as a *digital frequency divider* in half: every second pulse passes to the output of the circuit. It was shown [25] that on the basis of circuits with the described functionality, it is possible to implement logic elements, memory with destructive and nondestructive readout, RS and T flip-flops, half-adders, and more complex components of computing devices.

#### PHASE LOGIC CIRCUTS BASED ON $\pi$ JUNCTIONS

In [21, 33–36], it was demonstrated how the coexistence of 0 and  $\pi$  junctions allows obtaining a bistable  $\varphi$  junction. The key idea of this work is that the required bistable elements of the phase logic unit can be created by combining relatively easy-to-make 0 and  $\pi$  Josephson junctions. Figure 2 demonstrates a version of the basic logic unit, in which the phase converter  $J_v$  is made as a combination of 0 and  $\pi$  junctions ( $J_{0C}$  and  $J_{\pi C}$ ). The  $\pi$  structure can also be used as the central element of the unit  $J_m$ .

The total Josephson energy of the input cell, consisting of the junctions  $J_{in}$ ,  $J_{0C}$ ,  $J_{\pi C}$ , and  $J_m$ , as a function of the phase difference at the junctions  $J_{in}$  and  $J_m$ , has two local minima (see Fig. 3). It can be seen that the phase in stable states is equal to  $\pi + 2\pi n$  at  $\pi$  junctions and to  $2\pi n$  at 0 junctions, where *n* is an integer.

In this case, the input cell has an even number of  $\pi$  junctions, the total phase shift of the order parameter along the circuit is  $2\pi n$ , and there is no circulating current. This excludes unwanted feedback on the other units and allows one to conveniently connect phase logic circuits to standard FSQ logic elements. Note that a bistable input cell could be obtained without the use of  $\pi$  junctions, by introducing instead of them a large number of series-connected 0 structures that provide the phase shift of the order parameter.

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The output cell has an odd number of  $\pi$  junctions, so the difference between the phase  $J_m$  and the phase of 0 junctions creates a circulating current in it, which can flow in two directions, which allows one to read the state of the unit. This forces a drop in the phase of the order parameter  $\pi$  on the element  $J_l$ . It turns out that, for the stable operation of the circuit, it is optimal to implement such an element in the form of a stack consisting of three junctions  $J_{ll}-3$  connected in series.

To demonstrate the operability of all the key information processing modes listed above, the dynamic processes in the basic unit demonstrated in Fig. 2 are considered. When modeling the control processes and reading the state of the basic unit, the transmission lines consisting only of Josephson junctions will be considered [25]. The system of differential equations, taking into account the balance of currents for each node, was written within the generalized resistive model and was solved using the fourth and fifth order Runge–Kutta methods, as well as the Gauss method



**Fig. 3.** (Color online) Josephson energy of the input cell and the central element of the basic unit of phase logic on 0 and  $\pi$  junctions (in the frequency divider mode) versus the phases in  $J_m$  and  $J_{in}$  heterostructures. The stable logic states 0 and 1 for the system under consideration are highlighted. The critical currents of the  $J_{0C}$  and  $J_{\pi C}$  junctions are 1.2 and -0.35 of the critical current of the  $J_{in}$  junction, respectively. Normalized supply currents are  $i_b = 0.77$  and i = 0.4.



**Fig. 4.** (Color online) Phases on the junctions of the unit versus the time measured in units of  $\tau_C$  for the modes of (a) limiter mode at  $i_{\pi C} = -0.05$  and  $i_{0C} = 0.1$ , (b) transmission line at  $i_{\pi C} = -0.2$  and  $i_{0C} = 1.2$ , and (c) digital frequency divider at  $i_{\pi C} = -0.35$  and  $i_{0C} = 1.2$ . Normalized supply currents are shown in Fig. 3;  $\alpha_{0C} = 0.8$  and  $\alpha_{\pi C} = 0.9$ .

for solving systems of linear equations. For the *j*th Josephson junction in the unit, the equation of motion has the form

$$i_{\Sigma j} = i_{C j} \sin(\varphi_j) + \alpha_j \dot{\varphi}_j + \ddot{\varphi}_j, \qquad (1)$$

where  $i_{\Sigma j}$  is the total current flowing into the junction,  $i_{Cj}$  is the critical current, and  $\alpha_j$  is the damping factor. All currents are represented in units of the critical current of the input junction; the dot denotes the differentiation with respect to the time  $\tau$  measured in units of the characteristic time of the input junction  $\tau_c$ .



**Fig. 5.** (Color online) (Blue) limiter, (yellow) transmission line, and (cyan) frequency-halving operation modes of the basic unit of phase logic on 0 and  $\pi$  junctions on the plane of the junction parameters  $i_{\pi C}$  and  $i_{0C}$  of the phase converter in the input cell. Normalized supply currents and damping coefficients are the same as in Figs. 3 and 4.

Figure 4 demonstrates the time dependences of the phase on the junctions of the unit for the three modes, which occur after phase change waves sequentially reach the input.

Thus, in the *limiter mode* (Fig. 4a), when the critical current of the junction  $J_{\pi C}$  is slightly less than that of the junction  $J_{0C}$ , the  $\pi$  structure is the "weak point" in the input cell, at which a phase jump of ~ $2\pi$  occurs. In this case, the phases of the junctions  $J_m$  and  $J_{out}$  hardly change. In the *transmission line mode* (Fig. 4b), each phase change wave at the input changes the phase of the junctions  $J_m$  and  $J_{out}$  by  $2\pi$  and then propagates to the output transmission line. The pulses pass through the basic unit without changing its state: at the end of the calculation given for illustration,  $\pi + 8\pi$ . In the *frequency-halving mode*, each pulse at the input changes the phase of the junction  $J_m$  by  $\sim \pi$  (i.e., in this case,  $\varphi_1 \approx \pi$  and  $\varphi_2 \approx 2\pi$ ), but only every second pulse changes the phase of the junction  $J_{out}$  by  $2\pi$ .

It is possible to select the operating mode of the unit (limiter, transmission line, digital frequency divider) by selecting the critical currents  $i_{0C}$  and  $i_{\pi C}$  of the 0 and  $\pi$  junctions, respectively (Fig. 5). It is clearly seen that the limiter mode is implemented when switching between neighboring stable states in the phase converter in the input cell occurs earlier than in  $J_m$ . It can be seen from the equation of motion (1) that the rate of phase change at the junction is determined by the parameter  $\alpha_j$ . However, if the slow junction has a relatively low critical current, it may start switching earlier. For the frequency-halving mode, intermediate values of the speed of this element in the proposed phase logic unit are needed.



**Fig. 6.** (Color online) Time dependences of the normalized voltage,  $d\varphi/d\tau$ , at the (blue lines) input and (red lines) output of the basic  $\pi$  unit for (a) identical resistances of 0 and  $\pi$  junctions ( $\alpha_{0C} = 0.8$ ,  $\alpha_{\pi C} = 0.9$ , and  $\alpha_m = 1$ ), and (b) low resistances of  $\pi$  junctions ( $\alpha_{0C} = 0.8$ ,  $\alpha_{\pi C} = 9$ , and  $\alpha_m = 10$ ).

## PRACTICAL IMPLEMENTATION OF THE BASIC UNIT OF PHASE LOGIC ON $\pi$ JUNCTIONS

In practice, 0 Josephson junctions are usually superconductor-insulator-superconductor (SIS) tunnel heterostructures of the "sandwich" type. Compatible with FSQ circuits and quantum registers,  $\pi$  junctions are created in the form of superconductor-ferromagnet-superconductor (SFS) heterostructures with a sufficiently large critical current and a low resistance in the normal state [27, 28, 37, 38]. As a consequence, such  $\pi$  Josephson junctions have a low characteristic voltage and a low characteristic frequency [39–42]. Taking into account a low speed of  $\pi$  junctions in comparison with 0 junctions, we found that the operation of the cell is slowed. Figure 6 demonstrates that the duration of one working cycle of the circuit increases by a factor of about 1.5. In addition, the frequency-halving region on the plane of the junction parameters, which is a part of the phase converter, is narrowed (Fig. 5). This problem can be solved by switching to stacks, starting from the concept of a superconductor-insulator-superconductor-ferromagnet-superconductor (SIsFS) heterostructure.

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For such composite junctions, the characteristic voltage and frequency are of the same order as for tunnel Josephson junctions used in FSQ logic circuits [39–42].

The use of nanoscale (with an area of  $18000-30000 \text{ nm}^2$ ) Josephson junctions with a weak bond region made of a normal metal, constructed in the form of a bridge of variable thickness, is also promising [43, 44]. Since the functional geometric inductance is replaced by the Josephson one in the proposed basic unit, such a solution will provide a particularly notice-able gain in the compactness of the developed digital devices. Using this approach,  $\pi$  junctions can be obtained by using additional magnetic insulating layers in the weak-coupling region.

#### CONCLUSIONS

To summarize, a circuit has been proposed to implement the entire functionality of phase logic circuits without using bistable Josephson junctions [45], which are difficult to manufacture. At the same time, one of the key advantages of the approach under consideration, i.e., small planar dimensions of the circuits and, as a result, the possibility of achieving a high degree of integration for Josephson digital devices, can be retained. To reduce the planar dimensions of the proposed block, Josephson junctions (e.g., junctions  $J_{II-3}$  in the output cell) can be made in the form of a compact stack [46].

The planar size of the proposed basic unit can be estimated as the sum of the areas of all Josephson junctions of the circuit and the sum of the areas of connections between them. Under the assumption that the areas of all junctions are equal to S, and the same area is occupied by the connections, then the area of the basic unit is 14S. In the case of the MIT LL technology for superconductor-insulator-superconductor tunnel structures,  $S \approx 0.4 \ \mu m^2$  [47], and the area of the basic unit will be approximately  $5.6 \, \text{um}^2$ . In the case of a nanoscale Josephson junction with a weak bond region made of a normal metal, constructed in the form of a bridge of variable thickness [43], the required area is  $S \approx 0.018 \ \mu m^2$ , and the area of the basic unit is  $0.252 \,\mu m^2$ . The indicated marks make the prospects for the practical implementation of the Josephson phase logic circuit based on  $\pi$  junctions very relevant.

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## CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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