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Can HTS Josephson junctions be used for digital applications?

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Abstract.

We have analyzed HTS Josephson junctions on a subject to apply them to RSFQ digital circuits. The basic restriction on the HTS RSFQ circuit parameters are formulated. The main demands for the HTS Josephson junction fabrication processes are discussed as well as the possibility of using available types of the HTS junctions. The performed analysis shows that operating temperature can be about 40K for multylayer junctions and 10K for planar junctions. The most perspective types of Josephson junctions for HTS RSFQ are ramp junctions and electron beam writing junctions.

Introduction.

Recently it became obviously, that the future of superconductive digital electronics belongs to the types of Josephson logic based on nonhysteretic junctions [1]. The most promising of them is Rapid Single Flux Quantum (RSFQ) logic family [2].

At the present moment only Nb-AlOx-Nb technology process was successfully used to fabricate RSFQ circuits [3]. In order to provide nonhysteretic I-V characteristic of tunnel Nb-AlOx-Nb Josephson junctions the external resistive shunting has been applied. But external shunting of the tunnel junction decreases effective RnIc product, that leads to operation frequency reduction. The last investigations of HTSC Josephson junctions show their high RnIc product and nonhysteretic I-V characteristic [4-9]. With exception a number of works on three-layer junctions [10], High Temperature Superconductor (HTS) junctions are nonhysteretic. For this reason the logic families employing hysteretic junctions [1] cannot be used with HTS materials yet. Here we are going to discuss the possibility of the realization of RSFQ circuits using these junctions and set basic restrictions on HTS technology parameters.

Circuit parameters and basic requirements for fabrication process.

Most of RSFQ circuits have a basic three types of parameters, such as a critical current of junctions (Ic), an external DC bias current (Ib), and an inductance (L) (let us omit a few particular cases where junctions have different McCamber parameter).

The results of RSFQ circuit optimization show that the value of bias current Ib never exceeds 0.8 of critical current value Ic [11].

The lower band of the critical current value is estimated in order to keep the probability of the errors, induced by thermal noise, low enough. This probability is comparable with the probability of thermal activation of DC biased junction. The probability of thermal activation follows from [12]:

$\tau = 2\pi\omega_p^{-1}\exp(\varepsilon\gamma^{-1})$, where ω_p is plasma frequency,

$\varepsilon \cong \frac{4\sqrt{2}}{3}(1-\frac{I_b}{I_c})^{\frac{3}{2}}$ is normalized height of potential barrier, and $\gamma = \frac{2\pi\cdot kT}{\Phi_0 I_c}$ is the thermal noise coefficient.

For LSI circuits (with e.g. 10^4 Josephson junctions) operating at 100 GHz the resulting condition $\varepsilon\gamma^{-1} \le 100$ must be fulfilled in order to provide the error-free work during 10^4 seconds (3h). So for *Ib=0.8Ic* the critical current has to be

$$Ic[\mu A] \ge 8.4\cdot T[K]. \qquad (1)$$

It means, that at the liquid nitrogen temperature the minimal value of critical current has to exceed 0.65 mA.

The results of RSFQ circuit optimization show that for their proper work the following relation must be fulfilled:

$$L_{min} I_c \le \alpha\cdot\Phi_0, \qquad (2)$$

here *Lmin* is the minimal possible for given technology value of inductance of superconductive loop, and factor $\alpha \approx 0.1$ depends on circuit complexity. Combining the restrictions (1) and (2) one can easily obtain the dependence T_{max} versa L_{min} shown in the figure 1. The region below the curve corresponds to digital applicable fabrication process and cooling temperature.

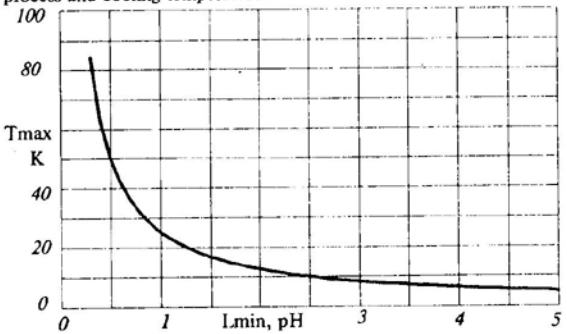

Figure 1

The most of existing HTS Josephson junction fabrication processes have one layer only [4,6,7]. In this case the loop is just a hole in YBCO thin film. The typical two-junction interferometer is showed in figure 2a. One can estimate the magnetic contribution into inductance of the hole as the inductance of the current loop: $L_m \approx p\,\mu_0/\pi$, where p is the perimeter of the current loop. The kinetic inductance of hole is roughly equal to $L_k \approx \mu_0\lambda_\perp^2\frac{p+4w}{w\cdot d}$, where w - current penetration depth, d - film thickness [13]. For the best fabrication parameters (p=8μ, w=2μ, $\lambda_\perp$=0.16μ, and d=0.2μ) at temperature less then 0.5 Tc the total inductance L≈4.5 pH (L_k≈1.3 pH, and L_m≈3.2 pH), that corresponds to maximum working temperature 5 K. One can significant reduce the magnetic contribution of loop inductance using ground plane (superconductor layer under the whole chip). It should be noted that the thickness of ground plane has to be as large as 2λ, that corresponds to 0.3-0.4 μ for YBCO films at temperatures below 40 K. Due to disorientation of c-axis the thickness of YBCO films in existing processes dose not exceed 0.2 μ. The numerical calculations show that in the given case ground plane placed under YBCO layer on a distance 0.2 μ reduces the L_m value up to 1 pH. So the limit of working temperature becomes 10K.

The other way to get rid of the large loop inductance is to use multylayer fabrication process, where the Josephson junction is placed between two layers [8,9]. Figure 2b shows two-junction interferometer with low loop inductance. The numerical calculations [14] for isolation layer thickness d=0.2 μ, width of junction w=2 μ, and distance between junctions l=5 μ yelled L_m≈0.4 pH. Taking into account relatively small value of penetration depth ($\lambda_\parallel$≈40 nm) the kinetic contribution one can estimate by formula $L_k \approx \mu_0\lambda_\parallel\cdot l/w \approx 0.2$ pH. And the total inductance value becomes L≈0.6 pH. Such low value of inductance allows us to work at 40 K.

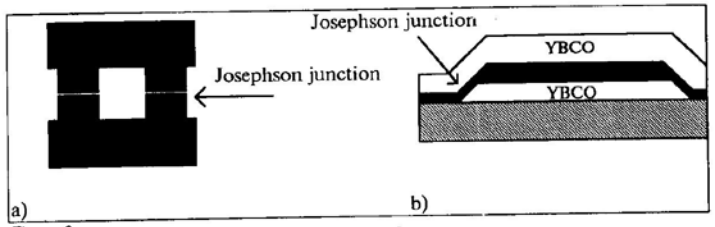

Figure 2

The mentioned above restrictions on critical current and inductance lead to corresponding requirements to fabrication process. In order to expand the feasible applications, and reduce total value of the inductance junction technology must be capable of integration into a multylayer circuit process.

HTS Josephson junctions fabrication processes.

At the present moment there is a number of methods for making Josephson junctions using HTS thin films. They include edge junctions with a variety of barrier materials, grain-boundary junctions (including bieepitaxial and bicrystal geometry), step-edge SNS junctions, and electron beam writing junctions.

In a multilayer circuit processes, whenever the YBCO film passes over patterned steps of the underlying film, its crystal structure can get distorted and grain boundary are initiated. For this reason it is difficult to use bieepitaxial and bicrystal junctions in LSI schemes. At present time only one example of the multilayer chip with SNS step-edge HTS Josephson junctions were demonstrated [5]. Nevertheless, due to the amout of attention attracted by this problem [15], progress has been quite fast, and some ways to solve it can be found. The current state of the HTS Josephson junction fabrication processes is shown in the Table 1.

Table 1

Type of the JJ	Ic (30K), μA	Uniformity	Ground plane	Multilevel
Bicrystall	500	5%	—	—
Step-edge	200	50%	—	—
Ramp	1000	*	+	+
SNS step-edge	300	5%	+	—
Electron beam writing	3000	*	+	—

* — *is not clear*

Discussion.

In comparison with earlier works [2,12], where overestimated requirements were set, theoretical analysis presented here shows that there are no fundamental restrictions to use HTS Josephson junctions in RSFQ digital devices. Moreover recently some of the RSFQ circuits on HTS Josephson junctions were designed and tested experimentally [16,18]. However, the performed analysis shows that operating temperature can be increased up to 10K saving correct operating of the RSFQ circuit. This restriction on the temperature follows from the principle requirements of RSFQ circuits and takes into account the present state of the HTS Josephson junction fabrication process. For the relatively simple structure of the circuits or after the solution the round plane problem this temperature can be increased up to 30K [17]. According to the Table 1 the ramp junctions, SNS step-edge junctions and electron beam writing junctions are more applicable for purpose of RSFQ design. For the higher operating temperatures the revision of the orthodox RSFQ principles has to be done.

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